3. (a) (i) What are the three transistor configurations? Draw the circuit diagram in each case for both *n-p-n* and *p-n-p* transistors.

(ii) What do you mean by DC load line and *Q*-point in case of transistor?

(iii) Draw a circuit diagram of transistor characteristics in CB configuration. Hence explain its current gain and input impedance.

(iv) In a common base connection $\alpha = 0{\cdot}55$, the voltage drop acroses 1 kΩ resistance connected in the collector circuit is 2V. Find the base current.

3+2+(2+2)+3=12

(OR)

(b) (i) What is voltage divider bias or self-bias? Draw the circuit diagram showing the self-bias of an *n-p-n* transistor in the CE configuration. Explain physically how the self-biasing resistor improves the stability.

(ii) What are the factors that affect the bias stability of a transistor? Define stability factor.

(iii) A CE amplifier uses a transistor with h_{ie} = 1kΩ, h_{fe} = 100, h_{re} = 5×10^{-4} and h_{oe} = $25\times10^{-6}\Omega^{-1}$. The load resistance is 5kΩ. Find the current amplification and input resistance.

(1+2+3)+(2+1)+3=12

3. (a) (i) Draw the output characteristic curves of an *npn* transistor in *CE* mode. Discuss about the different operating regions.

(ii) A transistor with $\beta = 75$ is connected in *CB* mode. What will be the maximum collector current for an emitter current $5\ mA$?

(iii) Establish the relation $I_C = \beta I_B + (1+B) I_{CBO}$ for *CE* transistor in active region.

Over

(iv) What are the differences among class - A, Class - B and Class - C Power amplifiers?

3+2+5+2=12

Or,

(b) (i) What is meant by stability of bias point of a transistor? Draw an emitter bias circuit and derive an expression of its stability factor.

(ii) Sketch the small signal low frequency hybrid parameter equivalent circuit of a transistor amplifier operating in the CE mode. Hence find the expression for input impedance and voltage amplification. (1+4)+(5+2)=12